AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (original) A nonvolatile semiconductor storage unit comprising:

a plurality of word lines;

a plurality of bit lines;

a plurality of memory cells each of which is correspondingly connected to one word line and one bit line and has a control gate and a floating gate;

a sense latch circuit which is connected to one end of said bit line and detects data on said bit line correspondingly to a threshold voltage for said memory cell;

a MOSFET which is connected between said bit line and said sense latch circuit, uses its gate to receive data on said bit line, and drives a node for said sense latch circuit;

a bit line precharge circuit which is connected to said bit line and precharges said bit line; and

a power supply circuit which is connected to said bit line precharge circuit and generates precharge voltage for said bit line dependently on a threshold voltage of said MOSFET.

2. (original) The nonvolatile semiconductor storage unit according to claim 1,

wherein said bit line precharge circuit can supply first and second potentials with different voltage values and further comprises a function to discharge said bit line,

wherein said bit line precharge circuit is supplied with said first potential when precharging said bit line, and

wherein said bit line precharge circuit is supplied with said second potential when discharging said bit line.

3. (currently amended) The nonvolatile semiconductor storage unit according to claim 2 further comprising:

a bit line selective precharge circuit which is connected to said bit line and selectively precharges said bit line,

wherein said bit line selective precharge circuit can supply third and fourth potentials with different voltage values and further comprises a function to determine data in said sense latch circuit in cooperation with said bit line precharge circuit,

wherein, when selectively precharging said bit line, said bit line selective precharge circuit is supplied with said third potential, and

wherein, when determining data in said sense latch circuit, said bit line selective precharge circuit is supplied with said ~~forth~~ fourth potential and said bit line precharge circuit is supplied with said second potential.

4. (original) The nonvolatile semiconductor storage unit according to claim 1 further comprising:

a selection circuit which is connected to a node of said sense latch circuit and interchanges data between said sense latch circuit and a common input/output line,

wherein said selection circuit can supply fifth and sixth potentials with different voltage values and

further comprises a function to precharge and discharge the node for said sense latch circuit,

wherein said selection circuit makes connection between said sense latch circuit and said common input/output line when data is exchanged therebetween,

wherein said selection circuit is supplied with said fifth potential when the node for said sense latch circuit is precharged, and

wherein said selection circuit is supplied with said sixth potential when the node for said sense latch circuit is discharged.

5. (currently amended) The nonvolatile semiconductor storage unit according to claim 1, ~~2, 3, or 4,~~

wherein said plurality of memory cells are commonly connected to a common line via a MOSFET whose source is driven by a gate control signal, and

wherein a gate of each memory cell is connected to each word line and a drain thereof is commonly connected to a bit line.

6. (currently amended) The nonvolatile semiconductor storage unit according to claim 1, ~~2, 3, or 4,~~

wherein each of said plurality of memory cells can store a plurality of bits of data as a threshold voltage.

7. (new) The nonvolatile semiconductor storage unit according to claim 2,

wherein said plurality of memory cells are commonly connected to a common line via a MOSFET whose source is driven by a gate control signal, and

wherein a gate of each memory cell is connected to each word line and a drain thereof is commonly connected to a bit line.

8. (new) The nonvolatile semiconductor storage unit according to claim 3,

wherein said plurality of memory cells are commonly connected to a common line via a MOSFET whose source is driven by a gate control signal, and

wherein a gate of each memory cell is connected to each word line and a drain thereof is commonly connected to a bit line.

9. (new) The nonvolatile semiconductor storage unit according to claim 4,

wherein said plurality of memory cells are commonly connected to a common line via a MOSFET whose source is driven by a gate control signal, and

wherein a gate of each memory cell is connected to each word line and a drain thereof is commonly connected to a bit line.

10. (new) The nonvolatile semiconductor storage unit according to claim 2,

wherein each of said plurality of memory cells can store a plurality of bits of data as a threshold voltage.

11. (new) The nonvolatile semiconductor storage unit according to claim 3,

wherein each of said plurality of memory cells can store a plurality of bits of data as a threshold voltage.

12. (new) The nonvolatile semiconductor storage unit according to claim 4,

wherein each of said plurality of memory cells can

store a plurality of bits of data as a threshold voltage.